What is claimed is:

1. A scheduling circuit comprising:

an IP (Internet Protocol) scheduling/format converting section for scheduling input IP packets and converting each of said IP packet to ATM (Asynchronous Transfer Mode) cells, said IP scheduling/format converting section including a plurality of packet FIFOs (First-In First-Out memories);

a plurality of cell FIFOs to each of which the ATM cells output from a corresponding one of said plurality of packet FIFOs are written; and

an ATM scheduling section for scheduling the ATM cells received from each of said cell FIFOs cell by cell.

2. The scheduling circuit as claimed in claim 1, wherein said ATM scheduling section calculates, while scheduling a given cell belonging to a given VCI (Virtual Channel Identifier), a logical transmission time for a next cell belonging to said VCI (Virtual Channel Identifier) and sends, if said next cell cannot be scheduled, an input inhibition signal to one of said plurality of cell FIFOs that has output said given cell.

3. The scheduling circuit as claimed in claim 2, wherein when any one of said plurality of packet FIFOs overflows, said IP scheduling/format converting section discards an entire packet.

4. The scheduling circuit as claimed in claim 3, wherein said ATM scheduling section comprises a VCI identifying circuit for identifying the VCI of each ATM cell by referencing a header attached to said ATM cell.

5. The scheduling circuit as claimed in claim 4, wherein said ATM scheduling section further comprises:

a logical transmission time memory for managing VCI numbers on the basis of a period of time;

a current time counter for outputting a current time;

a comparing/updating circuit for comparing the current time of an arrived cell and the logical transmission time;

a transmission time determining circuit for determining a transmission time of the cell; and

a conflict control memory for sending, in response to an output of said VCI identifying circuit, the ATM cell scheduled in accordance with the current time output from said current time counter and the transmission time determined by said transmission time determining circuit.

6. The scheduling circuit as claimed in claim 1, wherein said ATM scheduling section comprises a VCI identifying circuit for identifying the VCI of each ATM cell by referencing a header attached to said ATM cell.

7. The scheduling circuit as claimed in claim 6, wherein said ATM scheduling section further comprises:

a logical transmission time memory for managing VCI numbers on the basis of a period of time;

a current time counter for outputting a current time;

a comparing/updating circuit for comparing the current time of an arrived cell and the logical transmission time;

a transmission time determining circuit for determining a transmission time of the cell; and

a conflict control memory for sending, in response to an output of said VCI identifying circuit, the ATM cell scheduled in accordance with the current time output from said current time counter and the transmission time determined by said transmission time determining circuit.

8. The scheduling circuit as claimed in claim 1, wherein when any one of said plurality of packet FIFOs overflows, said IP scheduling/format converting section discards an entire packet.

9. The scheduling circuit as claimed in claim 8, wherein said ATM scheduling section comprises a VCI identifying circuit for identifying the VCI of each ATM cell by referencing a header attached to said ATM cell.

10. The scheduling circuit as claimed in claim 9, wherein said ATM scheduling section further comprises:

a logical transmission time memory for managing VCI numbers on the basis of a period of time;

a current time counter for outputting a current time;

a comparing/updating circuit for comparing the current time of an arrived cell and the logical transmission time;

a transmission time determining circuit for determining a transmission time of the cell; and

a conflict control memory for sending, in response to an output of said VCI identifying circuit, the ATM cell scheduled in accordance with the current time output from said current time counter and the transmission time determined by said transmission time determining circuit.

11. The scheduling circuit as claimed in claim 1, wherein said ATM scheduling section comprises a VCI identifying circuit for identifying the VCI of each ATM cell by referencing a header attached to said ATM cell.

12. The scheduling circuit as claimed in claim 11, wherein said ATM scheduling section further comprises:

a logical transmission time memory for managing VCI numbers on the basis of a period of time;

a current time counter for outputting a current time;

a comparing/updating circuit for comparing the current time of an arrived cell and the logical transmission time;

a transmission time determining circuit for determining a transmission time of the cell; and

a conflict control memory for sending, in response to an output of said VCI identifying circuit, the ATM cell scheduled in accordance with the current time output from said current time counter and the transmission time determined by said transmission time determining circuit.